outputting bits from the block interleavers in a row-wise manner in accordance with the selected predefined redundancy.

The Examiner states that Yagamuchi discloses coding, loading and outputting, but fails to explicitly disclose selecting a predefined redundancy. The Examiner states that "an encoder normally attaches a predefined amount of redundancy to data prior to transmission." The Examiner further identifies Tong as disclosing bits with a predefined redundancy. However Applicants again submit that Tang does not load bits in a column-wise manner and output bits from the block interleavers in a row-wise manner in accordance with the predefined redundancy.

Claim 8 recites:

A method of block puncturing for turbo code based incremental redundancy, the method comprising the steps of:

turbo coding an input data stream into systematic bits and parity bits;

loading the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner;

selecting a predetermined redundancy; and

mapping the bits from the systematic and parity block interleavers into a symbol mapping array in a row-wise manner in accordance with the selected redundancy, wherein the systematic bits are mapped into the upper rows of the array and the parity bits are mapped into the lower rows of the array.

The Examiner has not indicated where in Yagamuchi or Tong teaches "mapping the bits from the systematic and parity block interleavers into a symbol mapping array in a row-wise manner in accordance with the selected redundancy, wherein the systematic bits are mapped into the upper rows of the array and the parity bits are mapped into the lower rows of the array." Applicants fail to see where Yamaguchi alone or in combination with Tong shows or suggests the claimed invention.

Claim 14 recites:

A turbo coder with block puncturing for incremental redundancy, comprising:

a channel coder operable to code an input data stream into systematic bits and parity bits;

a first interleaver coupled to the channel coder, the first interleaver operable to load the systematic bits and parity bits into respective systematic and parity block interleavers in a column-wise manner;

a redundancy version selector coupled to the first interleaver, the redundancy version selector operable to select a predefined redundancy;

a bit priority mapper coupled to the redundancy version selector, the bit priority mapper operable to map bits from the block interleavers in a row-wise manner in accordance with the selected predefined redundancy.

Applicant's again submit that neither Yamaguchi nor Tang discloses "a redundancy version selector coupled to the first interleaver, the redundancy version selector operable to select a predefined redundancy; a bit priority mapper coupled to the redundancy version selector, the bit priority mapper operable to map bits from the block interleavers in a row-wise manner in accordance with the selected predefined redundancy."

Accordingly it is respectfully submitted that the application is in condition for allowance, and a Notice of Allowance is solicited.

Respectfully Submitted
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